Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of digital communication between two devices, said method comprising the steps of:

(1) a first device transmitting a predetermined bit pattern to a second device responsive to a start signal;

(2) said second device sampling for bits of said predetermined bit pattern at sampling times determined as a function of a delay period after said start signal;

(3) if said second device does not detect said predetermined bit pattern, increasing said delay period and repeating steps (1) and (2), and, if necessary, step (3);

(4) if said second device detects said predetermined bit pattern, setting the last delay period used in step (2) as a delay period to be used by said second device for sampling data for further transmissions from said first device to said second device; ~~and~~

(5) said second device using said last delay period for sampling further data transmissions from said first device to said second device; and,

wherein said second device performs step (2) twice before proceeding to steps (3) or (4).

2. (original) The method of claim 1 wherein said start signal is generated at said second device.

3. (original) The method of claim 1 wherein said start signal is a frame synchronization signal denoting a beginning of a frame.

4. (original) The method of claim 2 wherein said start signal is a frame synchronization signal denoting a beginning of a frame.

5. (original) The method of claim 1 wherein said start signal is transmitted on a first signal line, said predetermined bit pattern and all further data is transmitted on a second signal line and a clock signal is transmitted on a third signal line and wherein transmissions on said second signal line and said sampling times are also a function of said clock signal.

6. (currently amended) The method of claim 5 wherein said digital communication is ~~in accordance with the Active Communication Riser (ACR) Integrated Packet Bus (IPB) protocol~~ carried out under the control of a controller and is conducted between at least one target device.

7. (original) The method of claim 6 wherein said start signal and said clock signal are generated at said second device.

8. (currently amended) The method of claim 6 wherein said first device is one of said at least one target devices ~~a target device~~ and said second device is ~~an ACR~~ said controller.

9. (original) The method of claim 1 wherein step (1) is performed responsive to receipt of an instruction from said second device.

10. (original) The method of claim 5 wherein, in step (3), said delay is increased by one-half of a clock cycle.

11. (cancelled)

12. (currently amended) ~~The method of claim 1 further comprising the step of:~~ A method of digital communication between two devices, said method comprising the steps of:

(1) a first device transmitting a predetermined bit pattern to a second device responsive to a start signal;

(2) said second device sampling for bits of said predetermined bit pattern at sampling times determined as a function of a delay period after said start signal;

(3) if said second device does not detect said predetermined bit pattern, increasing said delay period and repeating steps (1) and (2), and, if necessary, step (3);

(4) if said second device detects said predetermined bit pattern, setting the last delay period used in step (2) as a delay period to be used by said second device for sampling data for further transmissions from said first device to said second device;

(5) said second device using said last delay period for sampling further data transmissions from said first device to said second device; and

(6) said first device predicting arrival of said start signal and commencing transmission of data in anticipation of receipt of said start signal.

13. (currently amended) A communication device for receiving digital data from another device, said communication device comprising:

a receive port for receiving data transmitted to said communication device from another device;

a processor adapted ~~to;~~ to:

(a) sample data received at said receive port for a predetermined bit pattern at sampling times determined as a function of a delay period after a start signal;

(b) if said communication device detects said predetermined bit pattern, setting the delay period last used in step (a) as a delay period to be used by said communication device for sampling data; and

(c) if said communication device does not detect said predetermined bit pattern, increasing said delay period and repeating step (a) and step (b) or (c); ~~and~~

(d) using said last delay period for sampling further data transmissions; and

wherein said processor performs step (a) twice before proceeding to steps (b) or (c).

14. (original) The communication device of claim 13 further comprising:

means for generating said start signal; and

a second port for transmitting said start signal to another device.

15. (original) The communication device of claim 13 wherein said start signal is a frame synchronization signal denoting a beginning of a frame.

16. (original) The communication device of claim 14 further comprising means for generating a clock signal; and

a third port for transmitting said clock signal to said other device and wherein transmission of said predetermined bit pattern and said sampling times also are a function of said clock signal.

17. (currently amended) The communication device of claim 16 wherein said digital communication is ~~in accordance with the Active Communication Riser (ACR) Integrated Packet Bus (IPB) protocol~~ carried out under the control of a controller and is conducted between at least one target device.

18. (currently amended) The communication device of claim 17 wherein said communication device is ~~an ACR~~ said controller ~~target device~~ and said other device is ~~an ACR~~ said target device.

19. (original) The communication device of claim 13 wherein said processor is further adapted to transmit an instruction to said other device, responsive to which said other device transmits said predetermined bit pattern.

20. (currently amended) A method of receiving digital communication, said method comprising the steps of:

(1) receiving from a transmit device a predetermined bit pattern;

(2) sampling for bits of said predetermined bit pattern at sampling times determined as a function of a delay period after a start signal;

(3) if said predetermined bit pattern is not detected, increasing said delay period and repeating steps (1) and (2), and, if necessary, step (3);

(4) if said predetermined bit pattern is detected, setting a last said delay period used in step (2) as a delay period to be used for sampling data for further transmissions from said transmit device; ~~and~~

(5) using said last delay period for sampling further data communications from said transmit device; and,

wherein said second device performs step (2) twice before proceeding to steps (3) or (4).

21. (new) A method of receiving digital communication, said method comprising the steps of:

(1) receiving from a transmit device a predetermined bit pattern;

(2) sampling for bits of said predetermined bit pattern at sampling times determined as a function of a delay period after a start signal;

(3) if said predetermined bit pattern is not detected, increasing said delay period and repeating steps (1) and (2), and, if necessary, step (3);

(4) if said predetermined bit pattern is detected, setting a last said delay period used in step (2) as a delay period to be used for sampling data for further transmissions from said transmit device;

(5) using said last delay period for sampling further data communications from said transmit device; and

(6) said transmit device predicting arrival of said start signal and commencing transmission of data in anticipation of receipt of said start signal.

22. (new) The method of claim 12 wherein said start signal is generated at said second device.

23. (new) The method of claim 12 wherein said start signal is a frame synchronization signal denoting a beginning of a frame.

24. (new) The method of claim 22 wherein said start signal is a frame synchronization signal denoting a beginning of a frame.

25. (new) The method of claim 12 wherein said start signal is transmitted on a first signal line, said predetermined bit pattern and all further data is transmitted on a second signal line and a clock signal is transmitted on a third signal line and wherein transmissions on said second signal line and said sampling times are also a function of said clock signal.

26. (new) The method of claim 25 wherein said digital communication is carried out under the control of a controller and is conducted between at least one target device.

27. (new) The method of claim 26 wherein said start signal and said clock signal are generated at said second device.

28. (new) The method of claim 26 wherein said first device is one of said at least one target devices and said second device is said controller.

29. (new) The method of claim 12 wherein step (1) is performed responsive to receipt of an instruction from said second device.

30. (new) The method of claim 25 wherein, in step (3), said delay is increased by one-half of a clock cycle.

31. (new) A communication system comprising a transmitting device and a communication device,

wherein said communication device comprises:

a receive port for receiving data transmitted to
said communication device from said transmitting device;
a receiver processor adapted to:
(a) sample data received at said receive port for a predetermined bit pattern at sampling times determined as a function of a delay period after a start signal;

(b) if said communication device detects said predetermined bit pattern, setting the delay period last used in step (a) as a delay period to be used by said communication device for sampling data; and

(c) if said communication device does not detect said predetermined bit pattern, increasing said delay period and repeating step (a) and step (b) or (c); and

(d) using said last delay period for sampling further data transmissions; and,

wherein said transmitting device comprises a transmitter processor adapted to predicting arrival of said start signal and commencing transmission of data in anticipation of receipt of said start signal.

32. (new) The communication device of claim 31 further comprising:

means for generating said start signal; and

a second port for transmitting said start signal to said transmitting device.

33. (new) The communication device of claim 31 wherein said start signal is a frame synchronization signal denoting a beginning of a frame.

34. (new) The communication device of claim 32 further comprising means for generating a clock signal; and

a third port for transmitting said clock signal to said transmitting device and wherein transmission of said predetermined bit pattern and said sampling times also are a function of said clock signal.

35. (new) The communication device of claim 34 wherein said digital communication is carried out under the control of a controller and is conducted between at least one target device.

36. (new) The communication device of claim 35 wherein said communication device is said controller and said other device is said target device.

37. (new) The communication device of claim 31 wherein said receiver processor is further adapted to transmit an instruction to said other device, responsive to which said other device transmits said predetermined bit pattern.